HTH9G09P900H(B)

900W, 1.8 - 900 MHz LDMOS Amplifier

Product datasheet

Description

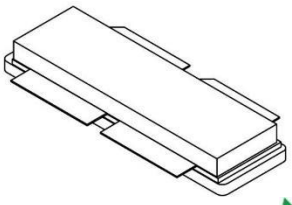
The HTH9G09P900H(B) is a discrete LDMOS Power Amplifier with 900W saturated output power covering frequency range from 1.8 - 900 MHz.

Features

- Operating Frequency Range: 1.8 - 900 MHz
- Operating Drain Voltage: 50V
- Saturation Output Power: 900W
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Internally integrated enhanced ESD design

Applications

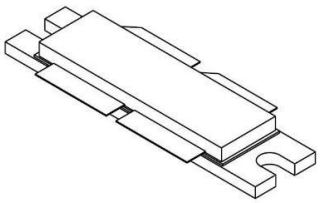
- Analog and Digital Broadcasting
- Meteorological and Aviation Radar
- Private network communication base station
- Industrial Laser Sources and Plasma Equipment
- Various nuclear magnetic resonance instruments
- Particle accelerator



ACC3210S-4L

Earless Flanged balanced Air Cavity Ceramic Package; 4 Leads

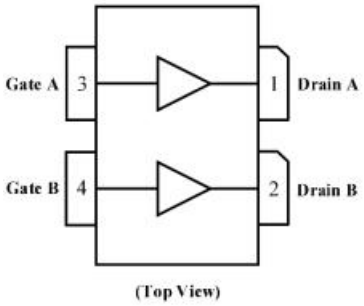
HTH9G09P900H



ACC3210B-4L

Flanged balanced Air Cavity Ceramic Package; 4 Leads,
2 Mounting holes

HTH9G09P900HB



Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Ordering Information

Part Number	Description
HTH9G09P900H(B)	Tray Package
HTH9G09P900H(B) EVB	470-700MHz EVB

Typical Performance

RF Characteristics (Pulsed CW)

Freq(MHz)	Gain(dB)	P5dB(dBm)	P5dB(W)	Eff(%)
470	20.52	59.13	818.46	57.90
500	23.24	59.37	864.97	58.39
550	22.14	59.38	866.96	56.19
600	20.08	59.41	872.97	57.36
650	20.78	59.07	807.24	55.71
700	20.15	59.02	797.99	53.29

Test conditions unless otherwise noted: 25 °C, VDD = +50dc, IDQ= 1000mA, PW = 100us, DC= 10% test on WATECH Application Board

RF Characteristics (Modulation)

Freq(MHz)	Gain(dB)	ACPR(dBc)	Eff(%)
470	20.06	-34.8	31.08
500	20.86	-34.2	31.83
550	19.18	-34.0	30.92
600	20.26	-34.2	31.17
650	19.93	-33.7	31.79
700	18.87	-32.9	30.63

Test conditions unless otherwise noted: 25 °C, VDD = +50dc, IDQ= 1150mA, Pout=52dBm（160W）Avg., Input signal PAR=9.9dB @0.01% Probability on CCDF test on WATECH Application Board

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5 to +110	V
Gate voltage (V_{GS})	-5 to +10	V
Storage Temperature (T_{STG})	-55 to +150	°C
Junction Temperature (T_J)	-40 to +225	°C

Electrical Specification

DC Characteristics (Carrier)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=424uA	110			V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=Vds, Ids=424uA	2.00	2.50	3.00	V

Drain Leakage Current I_{DSS}	Vgs=0V, Vds=50V	0	10	100	nA
Gate Leakage Current I_{GSS}	Vgs=5V, Vds=0V	0	5	100	nA

DC Characteristics (Peak)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=424uA	110			V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=Vds, Ids=424uA	2.00	2.50	3.00	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=50V	0	10	100	nA
Gate Leakage Current I_{GSS}	Vgs=5V, Vds=0V	0	5	100	nA

Load Mismatch Test

Condition	Test Result
VSWR=10:1 at all Phase Angles WCDMA: VDD=50V, IDQ=1000mA,, Freq=470MHz, Pout=250W Avg. test on WATECH Application Board	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE}= 25°C, V_{DD} = +50Vdc, I_{DQ}= 950mA, P_{AVG} = 52.2 dBm (166W), WCDMA signal	0.2	°C /W

Load Pull Performance Carrier

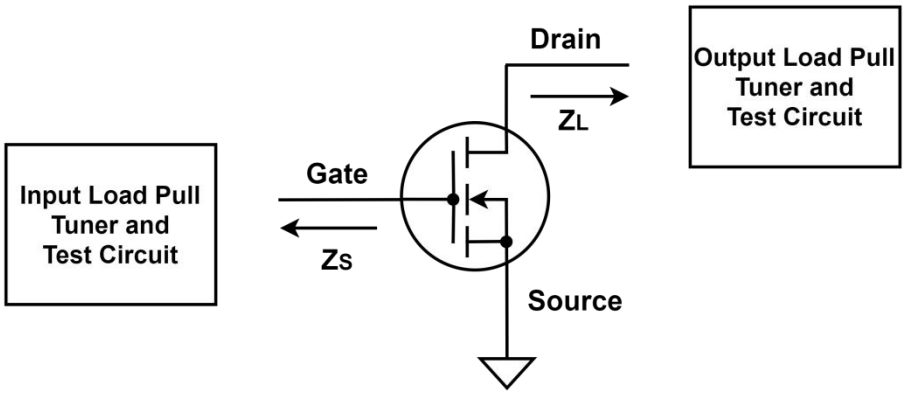
Test conditions unless otherwise noted: 25 °C, VDD = +50Vdc, IDQ= 500mA, PW = 100us, DC= 10%

Max Output Power						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	0.98-j*2.6	1.02+j*0.08	21.81	57.94	622.3	63.38

[1] Load impedance for optimum P3dB pout

Max Drain Efficiency						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	0.98-j*2.6	1.23+j*1.35	24.75	56.4	436.5	74.94

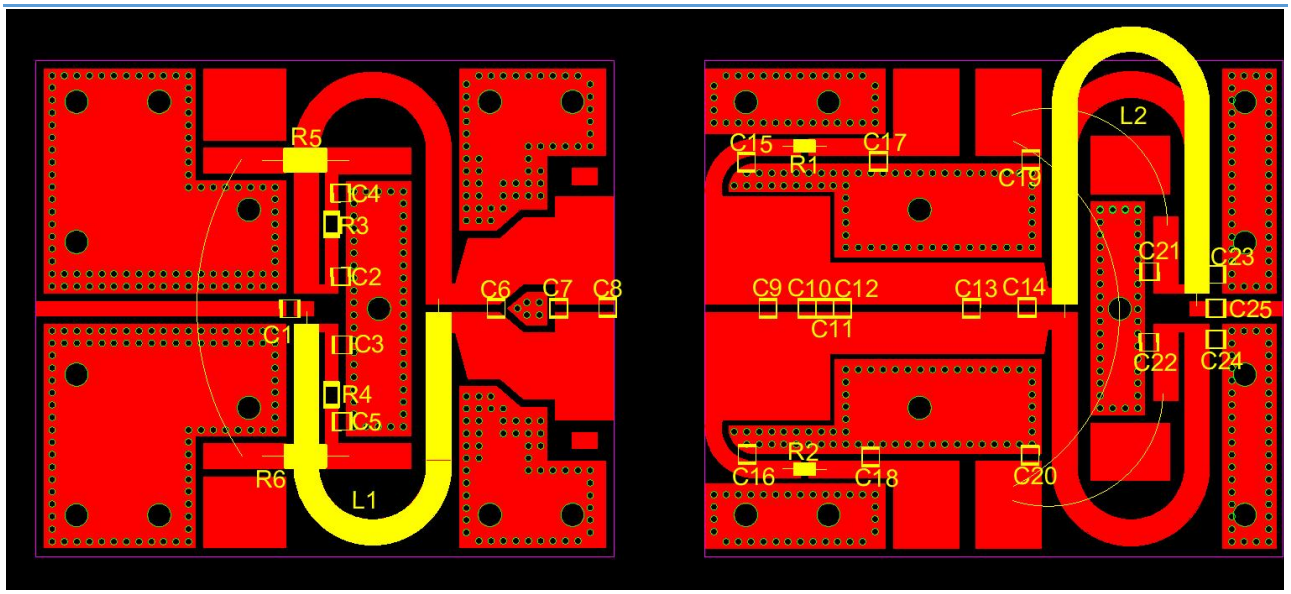
[2] Load impedance for optimum P3dB efficiency



Z_source : Measured impedance presented to the input of the device at the package reference plane

Z_load : Measured impedance presented to the output of the device at the package reference plane

HTH9G09P900H(B) 470-700 MHz Reference Design



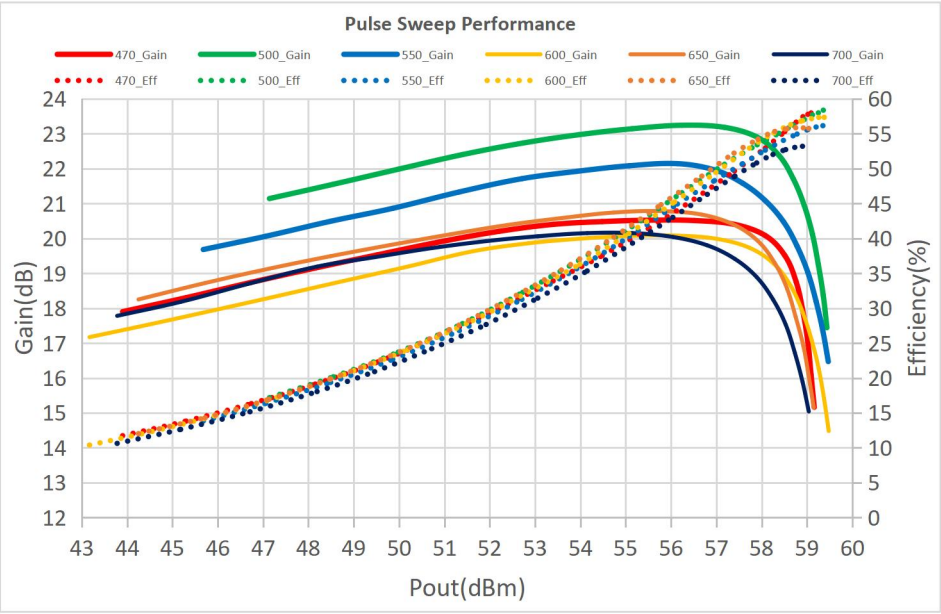
EVB Layout

Bill of Materials (BoM) - HTH9G09P900H(B) 470 - 700 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	900W, 1.8 - 900 MHz LDMOS Transistor	Watech	HTH9G09P900H(B)
C4,C5,C17,C18, C23， C24	10uF	100V Chip Capacitor	Murata	GRM32EC72A106KE05L
C6	20pF	Chip Capacitor	ATC	ATC100B200JT500XT
C1,C2,C3,C15,C	100pF	Chip Capacitor	ATC	ATC100B101JT500XT

16, C19,C20,C21,C22,C25				
C7	18pF	Chip Capacitor	ATC	ATC100B180JT500XT
C8	24pF	Chip Capacitor	ATC	ATC100B240JT500XT
C9	12pF	Chip Capacitor	ATC	ATC100B120JT500XT
C10,C11,C12	10pF	Chip Capacitor	ATC	ATC100B100JT500XT
C13	15pF	Chip Capacitor	ATC	ATC100B150JT500XT
C14	8.2pF	Chip Capacitor	ATC	ATC100B8R2JT500XT
R5,R6	100 Ω	Wire Resister		
R1,R2	11 Ω	Wire Resister		
R3,R4	6.2 Ω	SMD Resister		
L1	25 Ω 60mm 2:1	Balun		
L2	25 Ω 83mm 2:1	Balun		
PCB	RO4350 (er = 3.5), 30 mil (0.762 mm), 35 µm (1oz)			

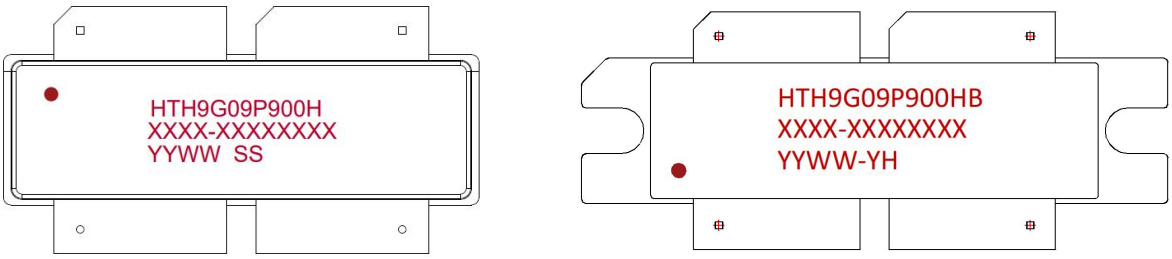
Performance Plots



Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +50Vdc, IDQ= 1000mA , PW = 100us, DC= 10% test on WATECH Application Board

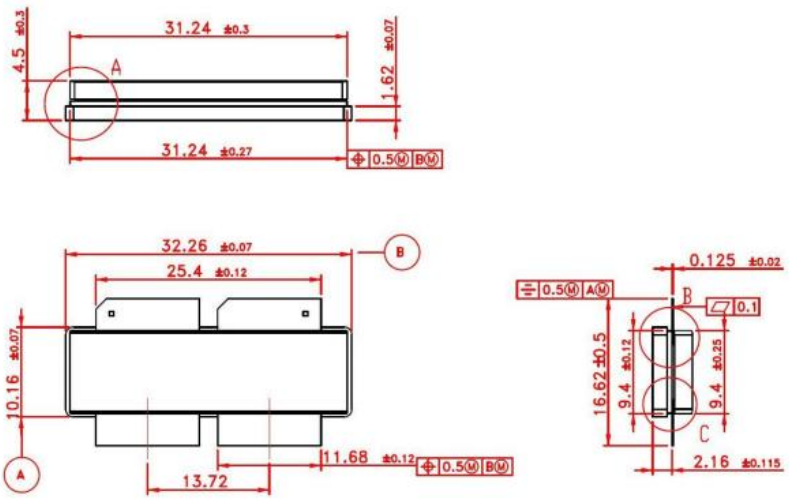
Package Marking and Dimensions



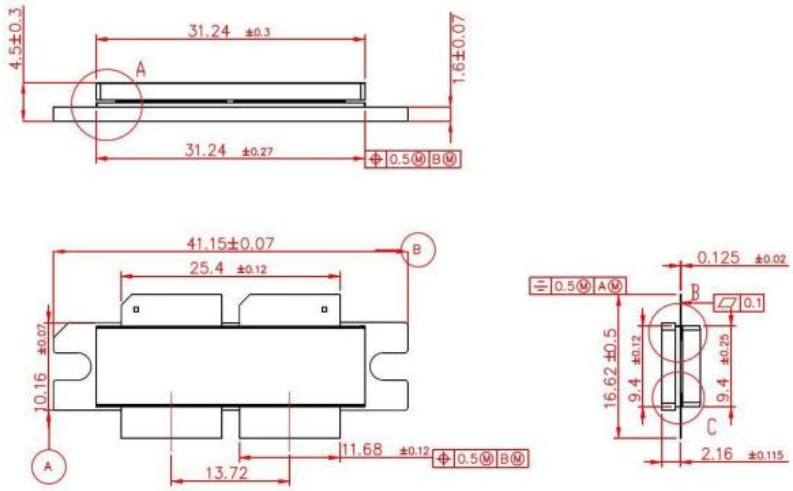
- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-EERA0001)
- Line3 (unfixed): Date Code+YH

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of “Watech Product Printing Specification”

Marking



ACC3210S-4L; Earless flanged balanced Ceramic Package; 4 Leads



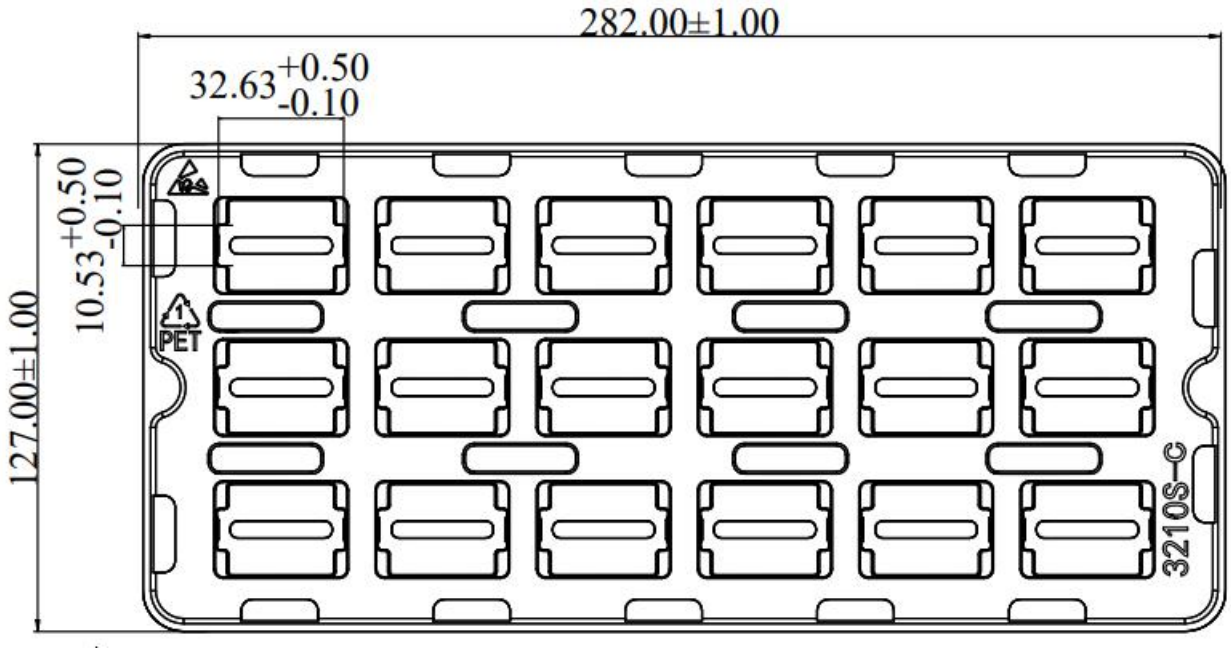
ACC3210B-4L; Flanged balanced Ceramic Package; 2 Mounting holes, 4 Leads

Package Dimensions

Packaging Information

HTH9G09P900H：

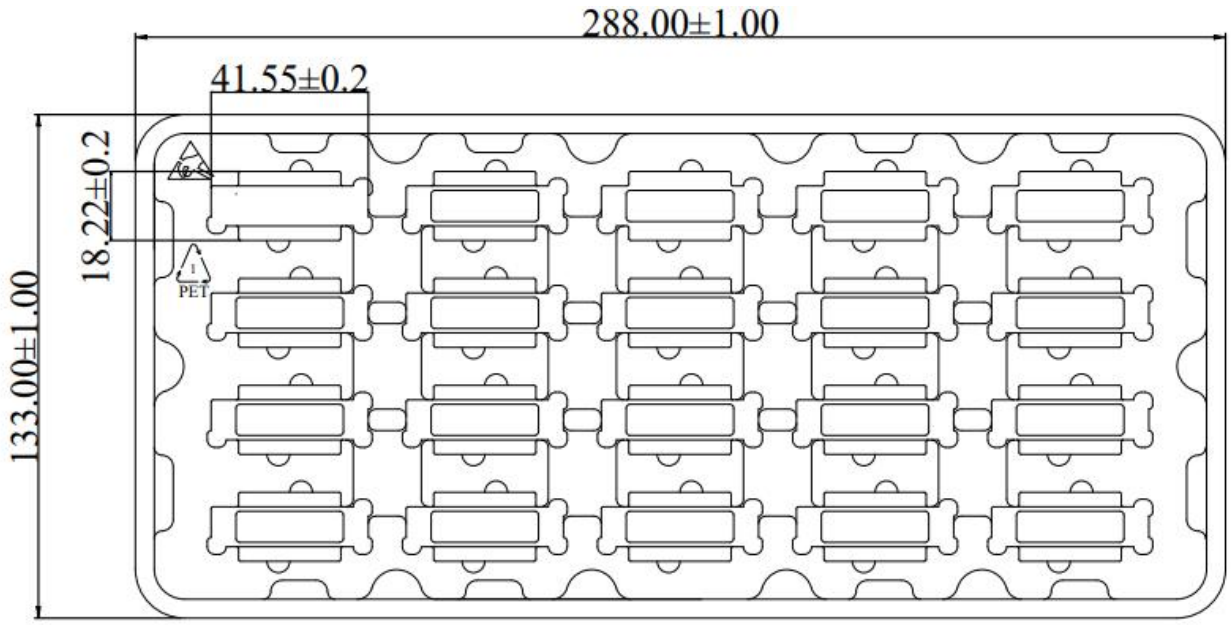
Package Type	Qty/Tray(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
ACC3210S-4L	18	90	540



Tray Packaging Descriptions

HTH9G09P900HB：

Package Type	Qty/Tray(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
ACC3210B-4L	20	100	600



Tray Packaging Descriptions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 1.0	Preliminary	Feb. 2022	Preliminary
Rev 2.0	Product	May. 2023	New format based on English version datasheet
Rev 2.1	Product	Sept. 2023	Update TBD information
Rev 2.2	Product	Dece. 2023	Update frequency information
Rev 2.3	Product	March 2024	Version released after re review

Contact Information

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